## REMARKS

In the non-final Office Action, the Examiner rejected claims 1-31 under 35 U.S.C. § 102(e) as anticipated by Kondo et al. (US Patent Publication No. 2003/0084218 A1).

By this Amendment, Applicant amends claims 8, 17, 23, and 27 to improve form. Applicant traverses the Examiner's rejection under 35 U.S.C. § 102 with regard to the claims as now amended. Claims 1-31 remain pending.

In paragraph 2 of the Office Action, the Examiner rejected claims 1-31 as allegedly anticipated by Kondo et al. Applicant traverses the rejection.

Claim 1, for example, recites a combination of features of a system for selecting bus mastership in a multi-master system. The system includes a plurality of master devices and at least one slave device. The master devices are configured to generate control signals relating to bus mastership in the multi-master system. The at least one slave device is/are configured to receive the control signals from the master devices, determine whether a conflict exists based on the control signals, generate one or more alternate control signals for selecting bus mastership when a conflict is determined to exist, and select bus mastership using the one or more alternate control signals.

A proper rejection under 35 U.S.C. § 102 requires that a single reference teach every aspect of the claimed invention either expressly or impliedly. Any feature not directly taught must be inherently present. See M.P.E.P. § 2131. Kondo et al. does not disclose or suggest each of the features recited in claim 1. For example, Kondo et al. does not disclose a plurality of master devices.

The Examiner alleged that Kondo et al. discloses a plurality of master devices and cited paragraph 0014 of Kondo et al. for support (Office Action, page 2). Applicant disagrees.

At paragraph 0014, Kondo et al. discloses:

> In order to accomplish the object, the present invention proposes by way of example a bus control method in an information processing system having a bus, and a plurality of modules connected to the bus, wherein a master which is the module having acquired mastership of the bus controls the bus and transfers an address and data to a slave which is the module being a transfer destination, in synchronism with cycles of a clock which is common to all the modules; comprising the step of allowing a specified one of the modules to acquire the bus mastership and so become master module; the step of allowing the master, having acquired the bus mastership, to execute a transfer cycle for transferring either of the address or the data to the slave, and to thereafter release the bus mastership; the step of allowing the module having received either of the transferred address and data as slave, to send all the other modules an acknowledge report indicating receipt of either of the address or the data, a predetermined number of cycles after the transfer cycle in which either the address or the data is transferred; and the step of allowing the module which executed the transfer as the master the predetermined number of cycles before the cycle in which the acknowledge report is sent, to verify success of the transfer in accordance with the sent acknowledge report.

In this paragraph, Kondo et al. defines a master as a module that has acquired mastership of the bus to transfer an address and data to a slave on the bus. In other words, Kondo et al. discloses that one of modules 100-107 can act as the master at any time and control address/data transfer on the bus (i.e., buses 50-60). Nowhere does Kondo et al. disclose or suggest multiple master devices.

Kondo et al. also does not disclose at least one slave device that, among other things, determines whether a conflict exists based on control signals from the master devices. Instead, Kondo et al. appears to disclose that bus arbiter 108 arbitrates bus mastership among modules 100-107 (para. 0035, 0046, and 0047).

The Examiner alleged that Kondo et al. discloses at least one slave device that determines whether a conflict exists based on control signals and cited paragraphs 0015 and 0037 of Kondo et al. for support (Office Action, page 2). Applicant disagrees.

At paragraph 0015, Kondo et al. discloses:

> According to the bus control method of the present invention, when the master has acquired the mastership of the bus, it executes the transfer cycle for transferring the address and the data to the slave, without checking the status of the slave, and it releases the bus mastership without verifying the success or failure of the transfer. On the other hand, the module having received the transferred address and data as the slave sends all the other modules the acknowledge report indicative of the receipt for each transfer cycle concerning the received address or data, the predetermined number of cycles after the corresponding transfer cycle. The module having executed the transfer as the master the predetermined number of cycles before the cycle in which the acknowledge report has been sent, verifies the success or failure of the transfer in the executed transfer cycle in accordance with the sent acknowledge report. Only when the transfer is not successful, is a countermeasure taken.

In this section, Kondo et al. merely discloses that a master transfers an address and data to a slave. Nowhere in this section, or elsewhere, does Kondo et al. disclose or suggest at least one slave device that determines whether a conflict exists based on control signals from the master devices, as recited in claim 1.

At paragraph 0037, Kondo et al. discloses:

> Regarding the system buses, the system bus 50 bears an address and data (A/D), and the system bus 51 bears a command signal (CMD) for designating the type of access. The system bus 52 bears an address valid signal (ADRV) indicating that the address on the address and data bus A/D (50) is valid, while the system bus 53 bears a data valid signal (DATAV) indicating that the data on the bus A/D (50) is valid. The system bus 54 bears a transaction acknowledge signal (TACK) with which a slave side notifies a master side of the fact that the address or the data has been correctly received. The system bus 55 bears a retry request signal (RETRY) which is directed from the slave side to the master side. The system bus 56 bears a synchronous error signal (SERR) being an error report signal which is synchronous with a transaction from the slave side to the master side, while the system bus 57 bears an asynchronous error signal (AERR) being an error report signal which is not synchronous with the transaction. The system bus 58 bears a freeze signal (FRZ) which is output simultaneously with the synchronous error signal SERR (56) or the asynchronous error signal AERR (57) so as to freeze any transaction other

> than a diagnostic transaction, while the system bus 59 bears a bus reset signal (BRST) which cancels the freeze signal after the information processing system has recovered from an error on the basis of the diagnostic transaction in the freeze operation. The system bus 60 bears a synchronizing clock signal (CLK) which is supplied to all the modules 100.about.107 in common.

In this section, Kondo et al. merely describes system buses 50-60. Nowhere in this section, or elsewhere, does Kondo et al. disclose or suggest at least one slave device that determines whether a conflict exists based on control signals from the master devices, as recited in claim 1.

Kondo et al. also does not disclose or suggest at least one slave device that, among other things, generates one or more alternate control signals for selecting bus mastership when a conflict is determined to exist, as further recited in claim 1. Instead, Kondo et al. appears to disclose that bus arbiter 108 arbitrates bus mastership among modules 100-107 (para. 0035, 0046, and 0047).

The Examiner alleged that Kondo et al. discloses at least one slave device that generates one or more alternate control signals for selecting bus mastership when a conflict is determined to exist and cited paragraphs 0015 and 0037 of Kondo et al. for support (Office Action, page 2). Applicant disagrees.

Paragraph 0015 of Kondo et al. has been reproduced above. In this section, Kondo et al. merely discloses that a master transfers an address and data to a slave. Nowhere in this section, or elsewhere, does Kondo et al. disclose or suggest at least one slave device that generates one or more alternate control signals for selecting bus mastership when a conflict is determined to exist, as recited in claim 1.

Paragraph 0037 of Kondo et al. has been reproduced above. In this section, Kondo et al. merely describes system buses 50-60. Nowhere in this section, or elsewhere, does Kondo et al.

disclose or suggest at least one slave device that generates one or more alternate control signals for selecting bus mastership when a conflict is determined to exist, as recited in claim 1.

For at least these reasons, Applicant submits that claim 1 is not anticipated by Kondo et al. Claims 2-7 depend from claim 1 and are, therefore, not anticipated by Kondo et al. for at least the reasons given with regard to claim 1. Claims 2-7 are also not anticipated by Kondo et al. for reasons of their own.

For example, claim 2 recites that the at least one slave device includes bus selection logic configured to determine whether the control signals indicate that two or more of the master devices concurrently assert bus mastership and generate a conflict indication signal when two or more of the master devices concurrently assert bus mastership, and conflict resolution logic configured to generate the one or more alternate control signals in response to the conflict indication signal. Kondo et al. does not disclose or suggest either of these features.

For example, Kondo et al. does not disclose or suggest at least one slave device that includes bus selection logic that determines whether the control signals indicate that two or more of the master devices concurrently assert bus mastership and generates a conflict indication signal when two or more of the master devices concurrently assert bus mastership. Instead, Kondo et al. appears to disclose that bus arbiter 108 arbitrates bus mastership among modules 100-107 (para. 0035, 0036, 0046, and 0047).

Kondo et al. also does not disclose or suggest at least one slave device that includes conflict resolution logic that generates the one or more alternate control signals in response to the conflict indication signal. Instead, Kondo et al. appears to disclose that bus arbiter 108 generates

a grant signal with which bus arbiter 108 grants a module 100-107 the use of system buses 50-60 (para. 0036).

The Examiner alleged that Kondo et al. discloses these features and cited paragraphs 0008, 0037, 0047, and 0052 of Kondo et al. for support (Office Action, page 3). Applicant disagrees.

At paragraph 0008, Kondo et al. discloses:

> In a case where one of the modules is to access another for a write operation by the use of the bus configured of such signal lines, the bus master first asserts the address valid signal ADRV indicating the validity of the address on the line A/D, and it simultaneously delivers the address of the access destination to the line A/D.

This section of Kondo et al. discloses nothing even remotely similar to the features recited in claim 2.

Paragraph 0037 of Kondo et al. has been reproduced above. In this section, Kondo et al. merely describes system buses 50-60. Nowhere in this section, or elsewhere, does Kondo et al. disclose or suggest the bus selection logic or the conflict resolution logic, as recited in claim 2.

At paragraph 0047, Kondo et al. discloses:

> As shown in the figure, the bus mastership request signals BREQ0.about.BREQ3 of the respective modules #0 (100).about.#3 (103) are simultaneously asserted. Herein, priority levels for the bus use are assumed to be higher in the order of the module #0 (100), module #1 (101), module #2 (102) and module #3 (103).

This section of Kondo et al. merely discloses that multiple bus mastership requests can be simultaneously asserted and that the order of priority is given by: module #0, module #1, module #2, etc. Nowhere in this section, or elsewhere, does Kondo et al. disclose or suggest at least one slave device that include the bus selection logic or the conflict resolution logic, as recited in claim 2.

At paragraph 0052, Kondo et al. discloses:

> The module having received the command and address of the read access acquires the bus mastership when it has prepared the response data. Thereafter, it asserts the data valid signal (DATAV) 53 indicating that the data on the address/data bus A/D is valid, and it delivers the response data to the address/data bus (A/D) 50. Simultaneously, it delivers the command signal to the bus (CMD) 51 to indicate that the type of access is a read response access. The response cycle of the read access is the seventh cycle in the figure.

This section of Kondo et al. discloses nothing even remotely similar to the features recited in claim 2.

For at least these additional reasons, Applicant submits that claim 2 is not anticipated by Kondo et al.

Claim 3 recites that the one or more alternate control signals include a bus switch signal that indicates whether a change in bus mastership is to occur and a bus select signal that indicates which of the master devices is to be granted bus mastership. Kondo et al. does not disclose or suggest these features. Instead, Kondo et al. appears to disclose a bus grant signal by which arbiter 108 grants module 100-107 the use of system buses 50-60 (paragraph 0036).

The Examiner alleged that Kondo et al. discloses these features and cited paragraph 0037 of Kondo et al. for support (Office Action, page 3). Applicant disagrees. Paragraph 0037 has been reproduced above. Nowhere in this section, or any other section, does Kondo et al. disclose or suggest the bus switch signal and the bus select signal.

For at least these additional reasons, Applicant submits that claim 3 is not anticipated by Kondo et al.

Claim 4 recites that the at least one slave device includes bus selection logic configured to determine whether the control signals indicate that none of the master devices asserts bus

mastership and maintain a previous bus mastership selection when none of the master devices asserts bus mastership. Kondo et al. does not disclose or suggest bus selection logic, as recited in claim 4.

The Examiner alleged that Kondo et al. discloses the claimed bus selection logic and cited paragraph 0037 of Kondo et al. for support (Office Action, page 3). Applicant disagrees. Paragraph 0037 has been reproduced above. Nowhere in this section, or any other section, does Kondo et al. disclose or suggest bus selection logic that determines whether the control signals indicate that none of the master devices asserts bus mastership and maintains a previous bus mastership selection when none of the master devices asserts bus mastership, as recited in claim 4.

For at least these additional reasons, Applicant submits that claim 4 is not anticipated by Kondo et al.

Amended independent claim 8 recites a combination of features of a system for selecting a master in a multi-master system. The system includes, among other things, means for generating a switch signal and a select signal when a conflict is determined to exist. Kondo et al. does not disclose or suggest this feature. Instead, Kondo et al. appears to disclose a bus grant signal by which arbiter 108 grants module 100-107 the use of system buses 50-60 (paragraph 0036). Kondo et al. does not disclose or suggest, however, the switch and select signals, as recited in amended claim 8.

For at least these reasons, Applicant submits that claim 8 is not anticipated by Kondo et al.

Independent claim 9 recites a combination of features of a method for selecting a bus in a multi-bus system. The method includes generating control signals relating to bus selection in the multi-bus system, determining whether a conflict for bus selection exists based on the control signals, generating one or more alternate control signals when a conflict is determined to exist, and selecting a bus using the one or more alternate control signals.

Kondo et al. does not disclose or suggest each of the features recited in claim 9. For example, Kondo et al. does not disclose generating control signals relating to bus selection in a multi-bus system. Instead, Kondo et al. treats buses 50-60 as a single bus when it comes to obtaining bus mastership (paragraph 0036). Kondo et al. does not disclose or suggest control signals relating to selection of a bus in a multi-bus system, as recited in claim 9. The Examiner did not address this feature and, therefore, did not establish a prima facie case of anticipation with regard to claim 9.

Kondo et al. also does not disclose or suggest selecting a bus using one or more alternate control signals, as further recited in claim 9. The Examiner also did not address this feature and, therefore, did not establish a prima facie case of anticipation with regard to claim 9.

For at least these reasons, Applicant submits that claim 9 is not anticipated by Kondo et al. Claims 10-16 depend from claim 9 and are, therefore, not anticipated by Kondo et al. for at least the reasons given with regard to claim 9. Claims 10-16 also recite features similar to the features described above with regard to claims 2-7. Claims 10-16 are, therefore, also not anticipated by Kondo et al. for reasons similar to those given with regard to claims 2-7.

Independent claim 18 recites a combination of features in a multi-master system having a plurality of master devices and a plurality of slave devices. Each of the slave devices includes

bus selection logic configured to determine whether control signals from the master devices indicate that two or more of the master devices concurrently assert bus mastership, generate a conflict indication signal when two or more of the master devices concurrently assert bus mastership, and select bus mastership using one or more alternate control signals when two or more of the master devices concurrently assert bus mastership, and conflict resolution logic configured to generate the one or more alternate control signals to identify bus mastership in response to the conflict indication signal.

Kondo et al. does not disclose or suggest each of the features recited in claim 18. For example, Kondo et al. does not disclose or suggest the bus selection logic or the conflict resolution logic, as recited in claim 18. When rejecting claim 18, the Examiner did not address either of the bus selection logic or the conflict resolution logic (Office Action, page 2). The Examiner did, however, address similar features when rejecting claims 2 and 11 (Office Action, page 3). Applicant traverses the Examiner's rejection for at least the reasons given above with regard to claim 2.

For at least these reasons, Applicant submits that claim 18 is not anticipated by Kondo et al. Claims 19-22 depend from claim 18 and are, therefore, not anticipated by Kondo et al. for at least the reasons given with regard to claim 18. Claims 19-22 also recite features similar to the features described above with regard to claims 2-7. Claims 19-22 are, therefore, also not anticipated by Kondo et al. for reasons similar to those given with regard to claims 2-7.

Amended independent claim 23 recites features similar to the features described above with regard to claim 1. Claim 23 is, therefore, not anticipated by Kondo et al. for reasons similar to those given with regard to claim 1. Claims 24-26 depend from claim 23 and are, therefore, not

anticipated by Kondo et al. for at least the reasons given with regard to claim 23. Claims 24-26 also recite features similar to the features described above with regard to claims 2-7. Claims 24-26 are, therefore, also not anticipated by Kondo et al. for reasons similar to those given with regard to claims 2-7.

Amended independent claim 27 recites features similar to the features described above with regard to claim 8. Claim 27 is, therefore, not anticipated by Kondo et al. for reasons similar to those given with regard to claim 8.

Independent claim 28 recites a combination of features of a multi-bus system. The system includes a plurality of buses; a plurality of master devices corresponding to the buses, each of the master devices controlling a corresponding one of the buses, the master devices generating control signals that indicate which of the buses is an active bus; and a plurality of slave devices connected to each of the buses and configured to receive the control signals, determine whether the control signals indicate that two or more of the buses are declared active buses, and select one of the buses when the control signals indicate that two or more of the buses are declared active buses.

Kondo et al. does not disclose or suggest each of the features recited in claim 28. For example, Kondo et al. does not disclose or suggest a plurality of master devices that correspond to a plurality of buses. Instead, Kondo et al. discloses that one of modules 100-107 can act as the master at any time and control address/data transfer on the buses 50-60 (para. 0036).

The Examiner alleged that Kondo et al. discloses this feature and cited paragraphs 0014 and 0037 of Kondo et al. for support (Office Action, page 5). Paragraphs 0014 and 0037 have

been reproduced above and neither of these sections, or any other section, of Kondo et al. discloses or suggests this feature.

Kondo et al. also does not disclose or suggest a plurality of slave devices that, among other things, select one of a plurality of buses. Instead, Kondo et al. treats buses 50-60 as a single bus when it comes to obtaining bus mastership (paragraph 0036). Kondo et al. does not disclose selecting one of buses 50-60.

The Examiner alleged that Kondo et al. discloses this feature and cited paragraphs 0014, 0035, and 0037 of Kondo et al. for support (Office Action, page 5). Applicant disagrees. Paragraphs 0014 and 0037 have been reproduced above and neither of these sections discloses or suggests selecting one of a plurality of buses, as recited in claim 28.

At paragraph 0035, Kondo et al. discloses:

> As shown in the figure, the information processing system in this embodiment comprises system buses 50.about.60, a plurality of modules #0.about.#7 (100.about.107) which are connected to the system buses 50.about.60, a bus arbiter 108 which arbitrates a bus mastership among the modules 100.about.107, an I/O (input/output) bus 110 which is connected to the modules 100.about.107, and I/O devices 111 and 112 which are connected to the I/O bus 110. In some cases, only one I/O device is connected to the I/O bus 110. Besides, a processor bus to which a CPU (central processing unit) and a memory are connected is connected to at least one of the modules 100.about.107. Each of the modules 100.about.107 includes therein a system bus interface device, which mediates the data transfer between the system buses 50.about.60 and the I/O bus 110 or the I/O device 111 or 112.

Nowhere in this section, or any other section, does Kondo et al. disclose or suggest selecting one of a plurality of buses, as recited in claim 28.

For at least these reasons, Applicant submits that claim 28 is not anticipated by Kondo et al. Claims 29-31 depend from claim 28 and are, therefore, not anticipated by Kondo et al. for at least the reasons given with regard to claim 28.

In view of the foregoing amendments and remarks, Applicant respectfully requests the Examiner's reconsideration of the application and the timely allowance of pending claims 1-31.

If the Examiner does not believe that all pending claims are now in condition for allowance, the Examiner is urged to contact the undersigned to expedite prosecution of this application.

To the extent necessary, a petition for an extension of time under 37 C.F.R. § 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account No. 50-1070 and please credit any excess fees to such deposit account.

Respectfully submitted,

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